Generating the test program for mixed-signal integrated circuits using the automata network

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ABSTRACT

Testing plays important role at early stages of implementation before mass production at detection the place and reason of violation in CUT operation. The checking and diagnostic tests are used in dependence of the testing purpose. The active application of the design-for-testability concept (DFT) is observed nowadays with rising the functional and structural complexity of the state-of-the-art IC, where the circuit development is realized simultaneously with the corresponding tests already at early stages of design process.

The effective test methods for digital IC have been developed and actively used now. In turn, the testing of analog circuits is related with the essential complexity due to absence the universal methods and necessity to develop and adapt test techniques for different classes of analog circuits or even for individual devices. Hence, the testing of the mixed-signal integrated circuits (MSIC) based on the joint test of digital and analog subcircuits is complex task requiring the matching of test methods used for both subcircuits.

An efficient generation of test programs ensuring comprehensive testing and diagnosis of MSIC, effective utilization of automated test equipment, reduction of time and money costs on test preparation and execution, etc. is one of the challenges in the area of mixed-signal testing.

The method of test program generation in the form of automata network providing the test execution with various resolving ability for MSIC using the automated test equipment is proposed.

The hierarchical testing ensuring the fault detection at the level of individual components, the functional blocks (FB), subcircuits or of the whole device is typically used at preparation and application the diagnostic tests.

Hierarchical testing of MSIC is aimed at test of analog subcircuits and its FB, digital subcircuits and its FB, converter circuits ADC and DAC, as well as the entire device on the whole. The circuit elements involved in the hierarchical testing form a set E. The testing process of MSIC is reduced to application the test signal to the input of the checked element and measuring the output responses based on which a decision on the correctness of the circuit operation is made, i.e. is possessed by the event nature. An algebraic automata theory is proposed for a description and synchronization the processes of MSIC test implementation. A finite-state machine is used for description the processes of testing the individual elements.

Two basic models for description the test process of MSIC in respect to hierarchical testing are proposed.

1) An automata network describing a set of independent parallel processes which provide testing the individual elements or FB of analog and digital subcircuits as well as converters.

2) An automata network describing a set of parallel processes ensuring the joint and matched in time testing of analog and digital functional blocks. The matching in time is realized by inclusion into the network additional synchronization conditions. The comprehensive testing of MSIC with application of test signals to the primary inputs of analog and digital subcircuits and responses acquisition at the primary outputs is a particular case of model 2.

The proposed method of test program generation in the form of automata network with a view of models considered above is described as the set of operations:

1. Prepare a set of input and output nodes of MSIC used at testing.

2. Describe the test methods for all elements of MSIC from the set E as finite state machines taking into account the features of circuit under test and the used test equipment.

3. Generate the matrix of MSIC nodes utilization during the testing for the set of constructed automatons.

4. For the model 1 define the set of independent processes in which there are no conflicts of nodes utilization during the testing.

5. Generate parallel automata network Net for the sets of independent processes ensuring the simultaneous testing of individual elements or FB analog and digital subcircuits as well as converters.

6. For the model 2 define the set of matched processes in which there are no conflicts of nodes utilization during the testing.

7. Generate automata network Net for the sets of matched processes ensuring the joint and matched in time testing of functional blocks analog and digital subcircuits. The generated network may possess a serial, parallel or